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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,694	01/23/2002	Chanchal Chatterjee	D02750	8890

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GENERAL INSTRUMENT CORPORATION DBA THE CONNECTED
HOME SOLUTIONS BUSINESS OF MOTOROLA, INC.
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EXAMINER

DO, CHAT C

ART UNIT	PAPER NUMBER
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2193

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/057,694	Applicant(s) CHATTERJEE, CHANCHAL	
	Examiner Chat C. Do	Art Unit 2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-28,43 and 44 is/are pending in the application.
- 4a) Of the above claim(s) 4-7 and 22-28 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16 and 17 is/are allowed.
- 6) ☒ Claim(s) 1,14,15,18-21,43 and 44 is/are rejected.
- 7) ☒ Claim(s) 8-13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>05/15/02</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This communication is responsive to Amendment filed 06/26/2006.
2. Claims 1-4, 28, and 43-44 are pending in this application. Claims 1, 16-17, and 43-44 are independent claims. In Amendment, claims 2-3, 29-42, and 45-46 are cancelled and claims 4-7 and 22-28 are withdrawn from consideration. This Office Action is made final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 14-15, 18-19, and 43-44 are rejected under 35 U.S.C. 103(a) as being obvious over Dijkstra (U.S. 6,795,841) in view of Sijstermans et al. (U.S. 6,889,242).

Re claim 1, Dijkstra discloses in Figures 2-3 a method in a signal processor for filtering samples in a digital signal (e.g. abstract), the method comprising: generating (e.g. Figure 3 with 32) an approximate filtered sample as a function of two samples (e.g. only two samples A or B in Figure 3) of the digital signal (e.g. only samples in term of A and B) wherein the two samples are a first fixed-point number, A (e.g. 26 in Figure 3), and a second fixed-point number, B (e.g. 28 in Figure 3), wherein generating the approximate filtered sample includes calculating $(A+B) \gg 1$ (e.g. output of 32 with right

shift by 1) wherein the ">>" represents a right-shift; generating a correction (e.g. 34 as A logically exclusive with B) as a function of the less than four samples (e.g. only samples in term of A and B); and generating a filtered sample (e.g. either 36 or 38 depending on the desirer) by modifying the approximate filtered sample with the correction (e.g. adding or subtracting 34). Dijkstra fails to disclose the adding 1 to the sum of A+B prior right shift. However, Sijstermans et al. disclose in Figure 4 a method of averaging of two number by summing inputs and adding another round factor as 1 and then right shift by one unit (e.g. adding 402, adding one 406, and right shift 404, and col. 6 lines 40-68). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a rounding factor as 1 to the sum of inputs prior right shift as seen in Sijstermans et al.'s Figure 4 into Dijkstra's invention because it would enable to increase degree of precision (e.g. col. 1 lines 31-35 and col. 1 lines 59-63).

Re claim 14, Dijkstra further discloses in Figures 2-3 the two samples are fixed-point numbers, and wherein generating the correction includes: calculating the correction as the exclusive OR (XOR) of the two samples; and masking the correction with the integer one (e.g. 34).

Re claim 15, Dijkstra further discloses in Figures 2-3 generating the correction further includes, prior to the masking step, generating a bit-wise complement of the correction (e.g. 34).

Re claim 18, Dijkstra further discloses in Figures 2-3 generating the filtered sample includes adding the correction to the approximate filtered sample (e.g. 38).

Re claim 19, Dijkstra further discloses in Figures 2-3 generating the filtered sample includes subtracting the correction from the approximate interpolated sample (e.g. 36).

Re claim 43, it is a computer program on computer readable medium claim of claim 1. Thus, claim 43 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 44, it is a system claim of claim 1. Thus, claim 44 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

5. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being obvious over Dijkstra (U.S. 6,795,841) in view of Sijstermans et al. (U.S. 6,889,242), as applied to claim 1 above, in further view of Intel ("IA-32 Intel^R Architecture Software Developer's Manual").

Re claims 20-21, Dijkstra in view of Sijstermans et al. do not disclose in Figures 2-3 the microprocessor is an Intel microprocessor with MMXTM/SSE, wherein the two samples are 8-bit fixed-point or integers numbers, wherein the steps of generating the approximate filtered sample, generating the correction and generating the filtered sample include executing the instructions:

```
{ pxor C REG, A REG ;  
pand C _REG, CONST;  
pavgb A REG, B REG ;  
psubb A REG, C REG ; }  
  
{ pxor C REG, A REG ;
```

```
pandn C_REG CONST;  
pavgb A_REG, B_REG ;  
paddb A_REG, C_REG ;}
```

wherein A-REG is a register that initially includes one of the two samples, B-REG is a register that includes the other of the two samples, C-REG is a register that initially includes the other of the two samples, and CONST is a constant that includes the eight-bit number 0x01. However, Intel discloses in pages 3-537, the microprocessor is an Intel microprocessor with MMXTM/SSE (e.g. pages 3-537), wherein the two samples are 8-bit fixed-point or integers numbers, wherein the steps of generating the approximate filtered sample, generating the correction and generating the filtered sample (e.g. averaging) include executing the instructions: pxor (e.g. pg 3-657), pand (e.g. pg 3-540), pavgb (e.g. pg 3-545), psubb (e.g. pg 3-630), pandn (e.g. pg 3-542), paddb (e.g. pg 3-529). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the intel microprocessor with all the instructions above as cited in Intel's manual into Dijkstra in view of Sijstermans et al.'s invention because it would enable to increase the system performance by utilizing pre-instructions in Intel processor.

Allowable Subject Matter

6. Claims 16-17 are allowed.

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7. Claims 8-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 06/26/2006 have been fully considered but they are not persuasive.

a. The applicant argues in page 12 third paragraph that the cited reference fails to disclose the limitation of the right shift because it only shifts the value $(A+B+1) \gg 1$ instead of $((A+B)-((AEORB)ANDMask)) \gg 1$.

The examiner respectfully submits that the claim does not define or require the correction factor is operated before or after the right shift. Thus, the right shift of $(A+B)$ with other correction factor would meet the limitation in the claimed invention.

b. The applicant argues in pages 13-14 first paragraph that the combination of references produces the exact same result as the original Dijkstra teachings and no added precision is gained as alleged by the Examiner.

The examiner respectfully submits that obviously the correction factor is already compensated for rounding error before shifting. Without the correction factor, adding one to the summation A and B before shifting would obviously improve the precision due shifting a odd number.

- c. The applicant argues in page 14 second paragraph that the cited reference fails to disclose the bit-wise complement as cited in the claimed invention.

The examiner respectfully submits that the $\sim(\text{AXORB})$ is equate to (AXNORB) .

The claim language does not require only one variable input as argued by the applicant. In conventional hardware operation, it is referable to operate logic device in untrue state due to power consumption.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

July 13, 2006


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